IMAGING IP-CORES

OVERVIEW

Revision 20140801-v01

www.helionvision.com

Helion
ENGINEERING VISION

IONOS-IMAGING IP-CORES

Overview

Helion's experience in image processing enables designers of video surveillance, automotive, and medical imaging systems to use pre-engineered high quality IP cores directly on their camera systems.

The IONOS Imaging IP Cores can be used for pre- and post-processing, image sensor control, FPGA algorithms and DSP algorithms.

Helion offers a comprehensive selection of video pipelines, ranging from basic to advanced monochrome and color pipelines, all the way through high resolution, advanced High Dynamic Range Imaging (HDRI) color pipelines.

These cores also support Lattice FPGA devices, and are all compatible and simply connected with the Wishbone bus as configuration port (versions without Wishbone are available on request).

Helion is a member of to the ispLeverCORE™ group of independent IP providers who have teamed up with Lattice to bring customers the highest quality, reusable IP cores optimized for Lattice's unique line of FPGA devices.

Features

- Supports image sensors up to 16MP resolution
  - Offers seamless upgrade path, protects investment
  - Direct sensor interfaces and setup
- 1080p60 streaming data path through FPGA
  - Supports full HD at 60 frames per second
  - No external frame buffer required
  - Offers quality at lower system cost
  - Extremely Low latency
- IP supports up to 192 dB (32Bit) scene dynamic range
  - Maximum details under difficult lighting conditions
  - Exceeds the 150dB automotive manufacturer
  - HDRI Tonemapping available
- Wishbone compatible IP and Mico32 support
  - Easy to setup and use
  - Double-click interconnect solution
  - Platform library and structure header files
- Comprehensive IP Suite
  - End to end ISP solutions

Revision 20140801-v01

Fast Time to Market with IONOS ISP

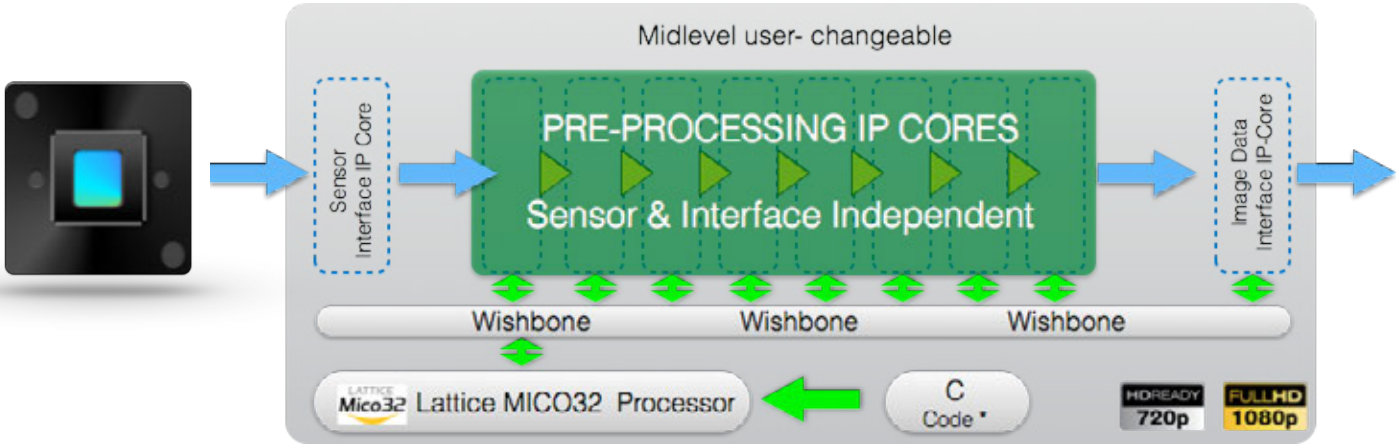
Helion offers a comprehensive selection of image processing pipelines, ranging from basic to advanced HDR-pipelines, which can be quickly evaluated on the Lattice HDR-60 camera development kit.

Containing more than 150 individual pieces of IP Cores, the library is available for licensing either entirely or in parts.

Overview of Imaging IP-Core Suite

DPC Defect Pixel Correction	TG Test Pattern	CSC Color Space Conversion	AC Aperture Correction
BLC Black Level Correction	AE Auto Exposure	AWB Automatic White Balance	LSC Lens Shading Correction
CFI Color Filter Interpolation	FRC Frame Rate Converter	HDRI High Dynamic Range Imaging	OI Output Interface
CCM Color Correction Matrix	LIN Linearisation	STAT Statistics	MI Memory Interface
Y Gamma Correction	NR Noise Reduction	OSD Overlay	SI Sensor Interface

Schematic of Signal flow



* Full configuration access, C-Code based IP

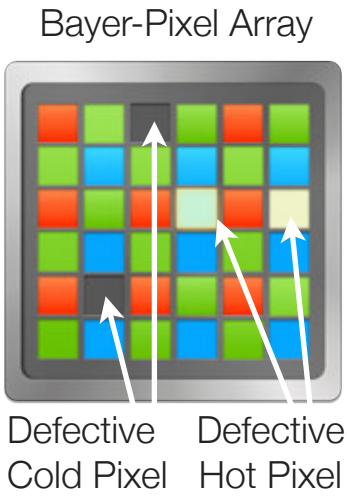
Revision 20140801-v01

Helion ENGINEERING VISION

DPC-Defective Pixel Correction

Description

Dead or hot pixels, are corrected with the defective pixel correction IP. This corrects the defective pixel with interpolated values based on neighbor pixels of the same color channel.



Goal

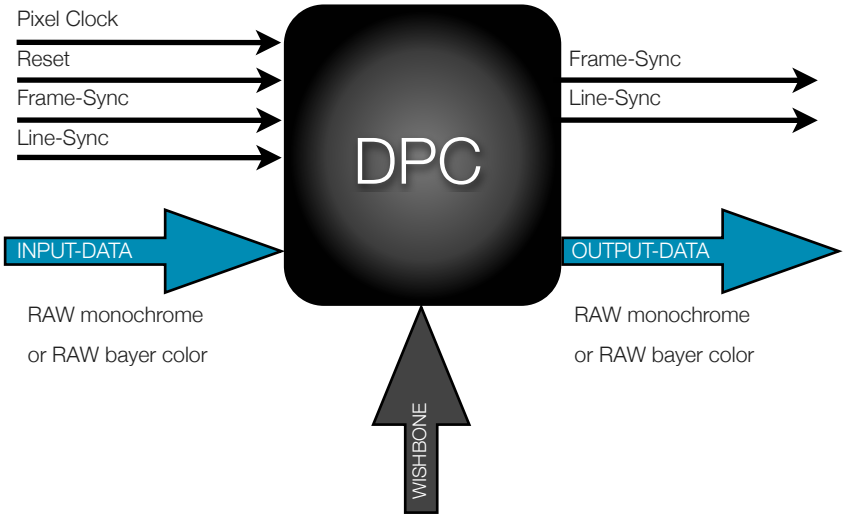
Typical correction methods include detection of cold or hot pixels using either median or averaging estimation on immediate pixel neighborhood.

IP-Features

- Selectable bit-width
(1..32Bit) for input pixel data, HDR/WDR ready

- Image resolution more than 16MP possible
- 1k, 2k, 4k, 8k line resolution version
- HD ready (720p/1080p)

- RAW monochrome (3x3) or RAW Bayer color (5x5) filter array
- Median or mean value filter version available
- Correct delay for sync signals - implied synchronization
- Reset-input to allow local or global reset
- Dynamic setup with wishbone-interface
    - extrapolation or skipping of picture border pixels
    - switch-off of complete module (bypass function)
    - ready to use platform library and structure header files for Mico32



Revision 20140801-v01

BLC- Black Level Correction

Description

Each color channel has a time dependent offset. Color processing requires linear signal behaviors. Therefore all signals must be without any offset. CMOS image sensors have a so called dark rows output to measure this average offset for each color channel.

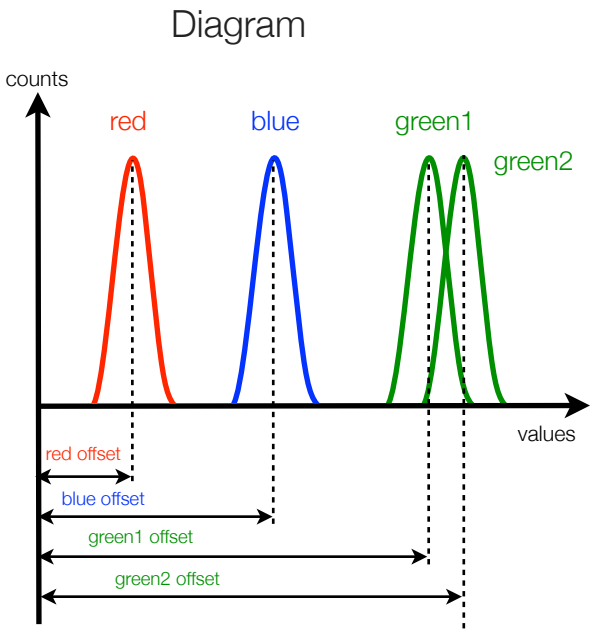
Goal

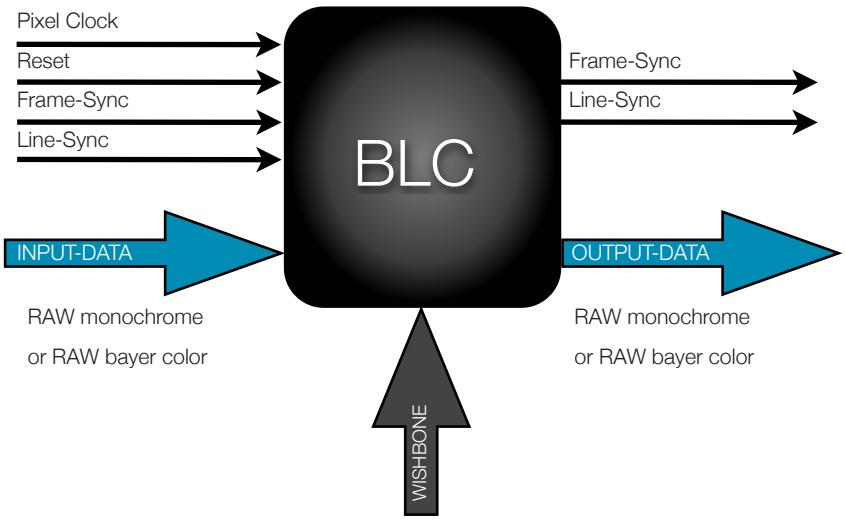
Subtraction of the color channel-specific, dark level offset, to achieve an optimal black level result.

IP-Features

- selectable bit-width (1..32Bit) for input pixel data, HDR ready
- image resolution more than 16MP possible
- HD ready (720p/1080p)
- Sync signal synchronization to image without black rows/columns reset
- each channel processed separately
- Dynamic Setup via wishbone-interface
    - adjustable integration time for black offset identification
    - selectable position of dark rows/columns

Diagram





Revision 20140801-v01

CFI- Color Filter Interpolation (Debayering)

Description

Since each pixel has a filter with one of three colors (R/G/B), two-thirds of the color data is missing from each. To obtain a full-color image, various demosaicing algorithms can be used to interpolate a set of complete red, green, and blue values for each pixel.

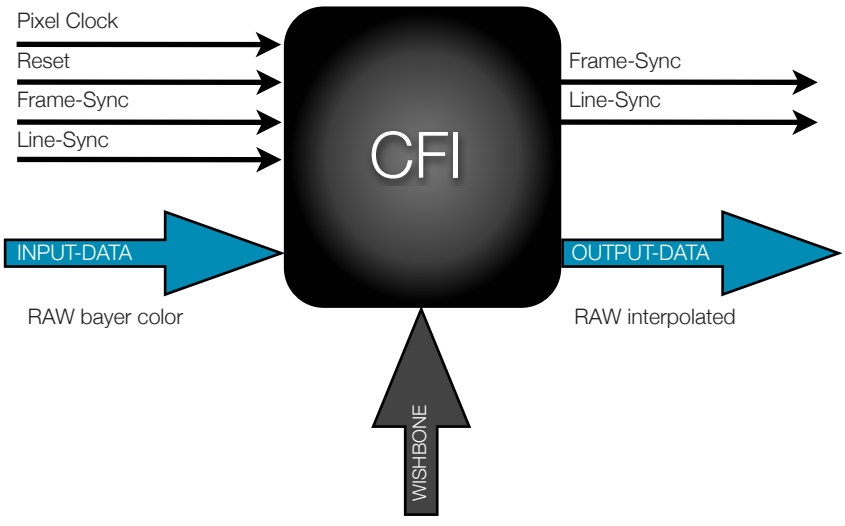
Bayer-Pixel Array

Goal

Full color information for each pixel of the sensor. Different versions are available.

IP-Features

- selectable bit-width (1..32Bit) for input pixel data, HDR ready
- image resolution more than 16MP possible
- HD ready (720p/1080p)
- Arbitrary picture size
- Reset input
- Sync signal synchronization
- 3x3 bilinear, 5x5 high-quality or 3x3 smart debayer with edge detection
- Dynamic setup with Mico32
- Border extrapolation
- Definition of first phase
- ready to use platform library and structure header files for Mico32



Revision 20140801-v01

Helion ENGINEERING VISION

CCM- Color Correction Matrix

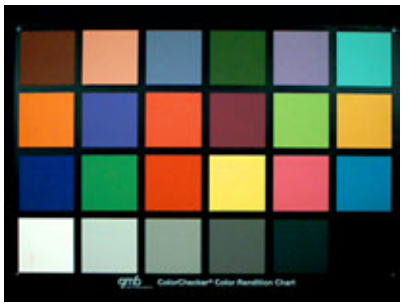
Description

In order to provide high quality images, acquisition is most important in respect to all further processing steps. A whole variety of current image sensors possess incorrect color rendition due to so called cross-color effects. This effects leads to wrong color images (e.g. green with too much blue).

Test Chart

D65

CCM



D65

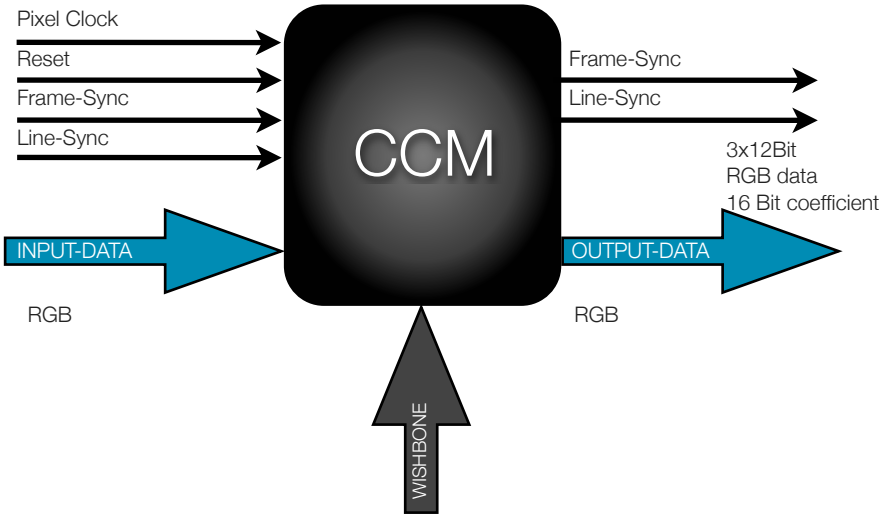
Goal

Modification of each single color channel by a 3x3 correction matrix.

red-out =rr*red+rg*green+rb*blue
green-out =gr*red+gg*green+gb*blue
blue-out =br*red+bg*green+bb*blue

IP-Features

- selectable bit-width (1..32Bit) for each color channel data, HDR ready
- image resolution more than 16MP possible
- HD ready (720p/1080p)
- 18 Bit coefficient with fixed point value
- Full color RGB in- and output
- Auto saturation detection
- Dynamic setup with wishbone interface
    - each matrix coefficient is a fix-comma number
    - switch off complete module (bypass function)
    - ready to use platform library and structure header files for Mico32



Revision 20140801-v01

Helion ENGINEERING VISION

γ- Gamma Correction

Description

Pixels are illuminated in a linear way. To provide pixel data to common video systems a conversion to a non-linear value encoding may be needed.

Goal

Conversion of a RGB-input signal from linear to non-linear value or otherwise under usage of arbitrary gamma correction factors.

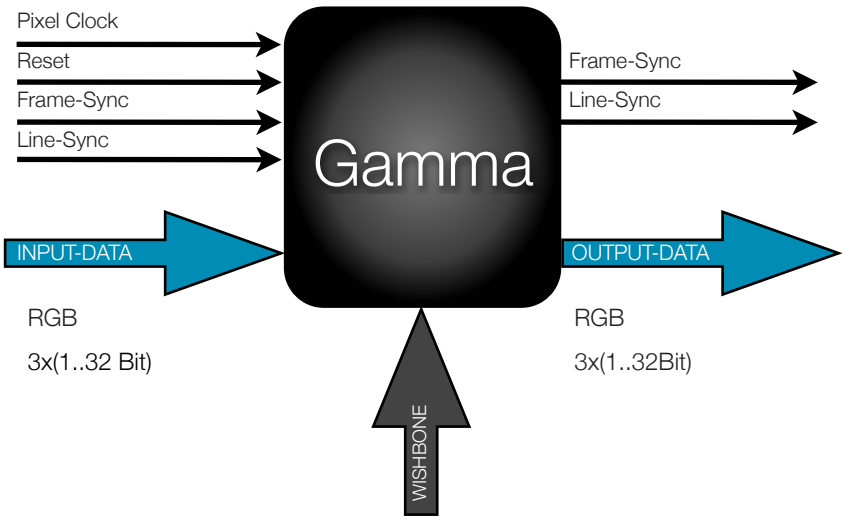
IP-Features

- selectable bitwidth (1..32Bit) for each color channel data, HDR ready
- image resolution more than 16MP possible
- HD ready (720p/1080p)
- selectable output data-width (for RGB)
- automatic interpolation between look up table entries (for use of smaller tables)
- for all colors, one look up table which is mapped into the wishbone address space
- Reset-input for global/local reset
- Separate correction for each single color channel
- Dynamic Setup via wishbone-interface
    - flexible modification of correction parameters
    - ready-to-use platform library and structure header files for Mico32
    - Gamma Compression or Gamma expansion possible to switch during processing

γ=1.0

CCM

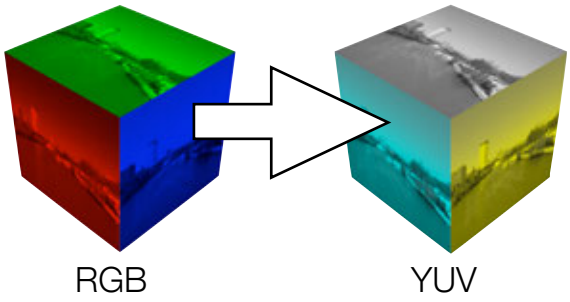
γ=0.5



Revision 20140801-v01

CSC- Color Space Conversion

Chroma up/down sampling



Description

Many processes need other input format then RGB. Especially data formats with decreased size, achieved by color downsampling are commonly used (e.g. encoders).

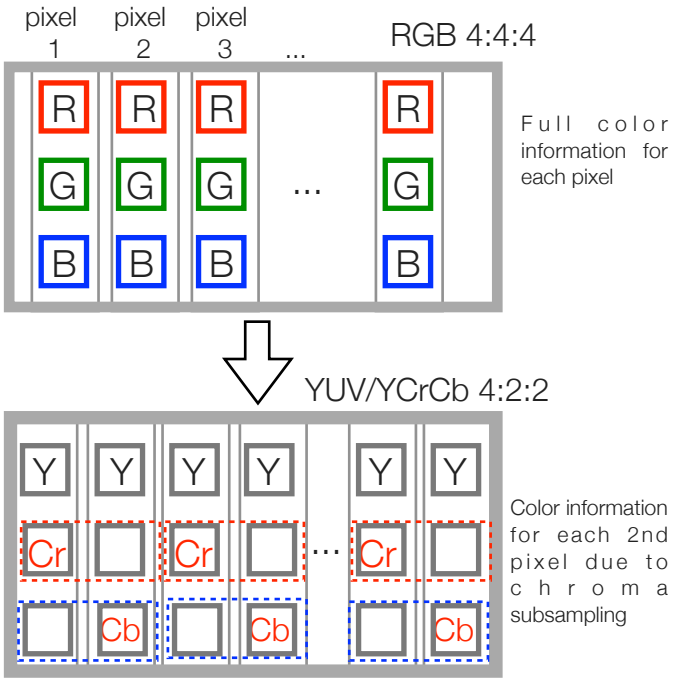
Goal

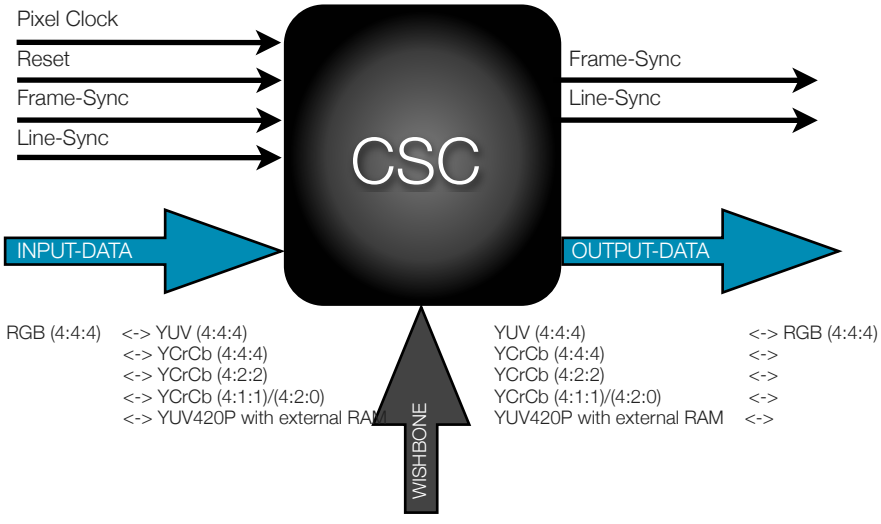
Conversion of picture stream data into different data formats.

IP-Features

- selectable bit-width (1..32Bit) for input pixel data, HDR ready
- image resolution more than 16MP possible
- HD ready (720p/1080p)
- Sync signal synchronization
- planar or interleaved data formats
- selectable output formats:
  - RGB->YUV420P, YCrCb422
- Color space calculation and color up/down sampling
- dynamic setup with wishbone-interface
  - extrapolation or skipping of picture border pixels
  - switch-off of complete module (bypass function)
  - ready to use platform library and structure header files for Mico32
  - Output data sorting
  - YCrCb output format adjustment

Data stream with RGB values for each pixel.





Revision 20140801-v01

Helion ENGINEERING VISION

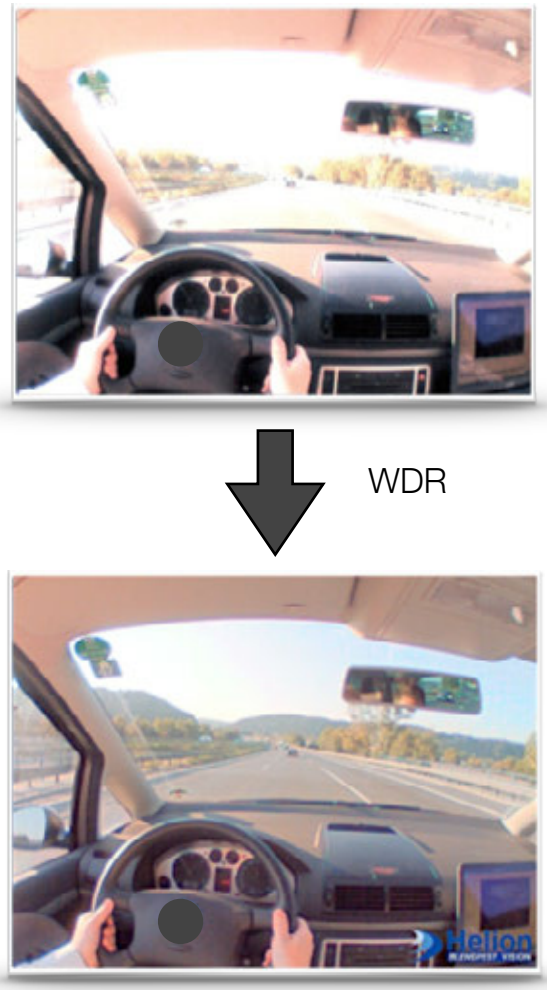
WDR- Wide Dynamic Range Tone-mapping

Description

Fully configurable comprehensive High Dynamic Range (HDR) pipeline, works with industry standard HDR sensors, and delivers outstanding HDR performance in one of the industry's most innovative FPGA based HDR implementations.

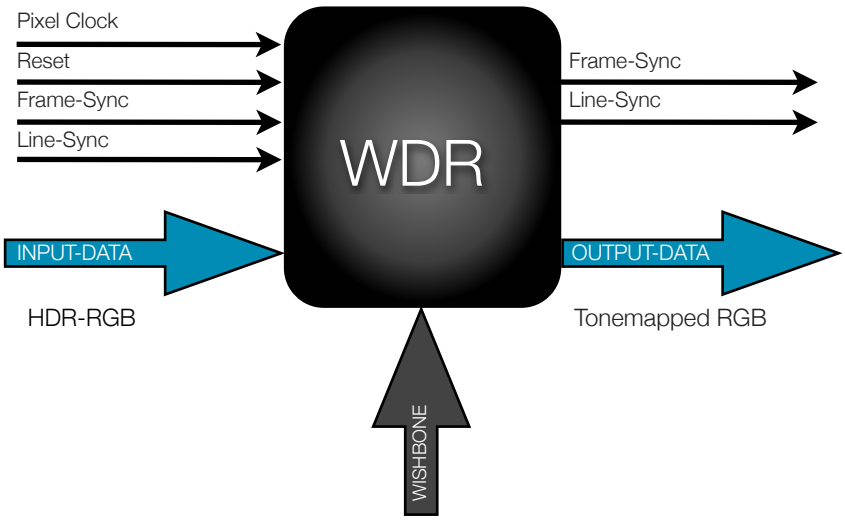
Goal

Extremely wide 120dB-HDR-IP ensures that no detail in dark areas is lost even when an intruder shines a flashlight directly into the camera lens, while HDR, working in close conjunction with a fast-auto-exposure rapidly adjusts exposure in changing light conditions to offer a system dynamic range of 170dB (sensor dependent).



IP-Features

- selectable bit-width (1..32 Bit) for each color channel
- selectable output bit-width
- image resolution more than 16MP possible
- HD ready (720p/1080p)
- no external memory needed
- Brightness dependent tone-mapping
- transfer curve fully configurable
- linear mapped into Wishbone address space



Revision 20140801-v01

IP Suite Overview

Pos.	List of IP-Blocks	Wishbone	Standalone	Mico32	Bits per Color	Resolution	Reference Design	Custom Projects
1	Color Interpolation, 3x3 Bilinear Debayer	x	x		8/10/12/16/20/32	1k/2k/4k/8k		x
2	Color Interpolation, 3x3 Smart Debayer	x	x		8/10/12/16/20/32	1k/2k/4k/8k	x	x
3	Color Interpolation, 5x5 HQ Debayer	x	x		8/10/12/16/20/32	1k/2k/4k/8k	x	x
4	Color Interpolation, double 3x3 HQ Debayer	x	x		8/10/12/16/20/32	1k/2k/4k/8k	Q4/14	x
5	CCM Color Correction Matrix	x	x		8/10/12/16/20/32		x	x
6	CCM Color Saturation Matrix	x	x		8/10/12/16/20/32		x	x
7	Luminance Adaptive Color Desaturation	x	x		8/-/-/-/-/-		x	x
8	Gamma Correction	x	x		8/10/12/16/20/32		x	x
9	Gamma Correction with linear interpolation	x	x		8/10/12/16/20/32		x	x
10	Mono gain, 16.16 Bit fixed point gain	x	x		8/10/12/16/20/32		x	x
11	RGB gain, 16.16 Bit fixed point gain	x	x		8/10/12/16/20/32		x	x
12	2 channel mixer with 256 mixing stages		x		8/10/12/16/20/32			x
13	Pixel Clock Detector		x					x
14	Green-Channel Balancing			x				
15	AWB Automatic White Balance			x			x	x
16	3D Noise Reduction (external RAM needed)	x	x		8/10/12/16/20/32	1k/2k/4k/8k	Q3/14	x
17	2D Noise Median Filter	x	x		8/10/12/16/20/32	1k/2k/4k/8k	x	x
18	2D Defect Correction on the Fly	x	x		8/10/12/16/20/32	1k/2k/4k/8k	x	x
19	1D Defect Correction on the Fly	x	x		8/10/12/16/20/32	1k/2k/4k/8k		x
20	Lensshading Correction (one channel, e.g. Luminance)	x			8/10/12/16/20/32	1k/2k/4k/8k		x
21	Lensshading Correction (three channel, e.g. RGB)	x			8/10/12/16/20/32	1k/2k/4k/8k		x
22	Generic Filter Kernel with 3x3 user matrix	x	x		8/10/12/16/20/32	1k/2k/4k/8k		x
23	Delay line		x		8/10/12/16/20/32	1k/2k/4k/8k		x
24	3x3 delay line core		x		8/10/12/16/20/32	1k/2k/4k/8k		x
25	5x5 delay line core		x		8/10/12/16/20/32	1k/2k/4k/8k		x
26	Full pipelined divider		x		8/10/12/16/20/32			x
27	Aperture Filter with selectable Strength	x	x		8/10/12/16/20/32	1k/2k/4k/8k	x	x
28	Sobel Filter	x	x		8/10/12/16/20/32	1k/2k/4k/8k	x	x
29	Global Motion Vector Estimation	x	x		8/10/12/16/20/32	1k/2k/4k/8k		x
30	AE Fast Auto Exposure, LDR-Fast-AE			x			x	x
31	AE Iterative Linear Auto Exposure, LDR-AE			x			x	x
32	AE High Dynamic Range Fast Auto Exposure HDR-Fast-AE			x			x	x
33	AE Antiflicker Option for LDR-AE and HDR-AE			x			x	x
34	Sensor specific AE for MT9M024 in HDR mode			x			x	x
35	Sensor specific AE for MT9M024 in linear mode			x			x	x
36	Sensor specific AE for AR0331 in HDR mode			x				
37	Sensor specific AE for AR0331 in linear mode			x			x	x
38	Sensor specific AE for MN34041 in linear mode			x			x	x
39	Sensor specific AE for IMX104/136/236 in HDR mode			x				
40	Sensor specific AE for IMX104/136/236 in linear mode			x			x	x
41	Sensor specific AE for VITA1300 in linear global-shutter mode			x			x	x
42	BLENDFEST HDRI V1 (gain based) monochrom (up to 32 bit)	x			-/-/-/16/20/32			
43	BLENDFEST HDRI V1 (gain based) color (up to 32 bit per color channel)	x			-/-/-/16/20/32			x
44	BLENDFEST HDRI V2 (ratio based) monochrom (up to 32 bit)	x			-/-/-/16/20/32			
45	BLENDFEST HDRI V2 (ratio based) color (up to 32 bit per color channel)	x			-/-/-/16/20/32		x	x
46	Framerate Converter (30fps->60fps + ext. SRAM)		x		8/-/-/-/-/-	1k/2k/4k/8k		x
47	Color Space Conversion with downsampling (24 Bit RGB (4:4:4) -> 16 Bit YCr YCb (4:2:2))		x		8/-/-/-/-/-	1k/2k/4k/8k		x
48	Color Space Conversion with upsampling (16 Bit YCr YCb (4:2:2) -> 24 Bit RGB (4:4:4)		x		8/-/-/-/-/-	1k/2k/4k/8k		x
49	Color Space Conversion (24 Bit RGB (4:4:4) -> 24 Bit YCrCb(4:4:4)		x		8/-/-/-/-/-	1k/2k/4k/8k		x
50	Color Space Conversion (24 Bit YCrCb (4:4:4) -> 24 Bit RGB (4:4:4)		x		8/-/-/-/-/-	1k/2k/4k/8k		x
51	Color Space Conversion with downsampling (Bit RGB (4:4:4) ->YUV420P (4:2:0)) + ext. RAM		x		8/-/-/-/-/-	1k/2k/4k/8k		x
52	Color Space Conversion witgh upsampling (YUV420P (4:2:0) -> RGB (4:4:4)) + ext. RAM		x		8/-/-/-/-/-	1k/2k/4k/8k		

Revision 20140801-v01

Helion ENGINEERING VISION

IP Suite Overview

Pos.	List of IP-Blocks	Wishbone	Standalone	Mico32	Bits per Color	Resolution	Reference Design	Custom Projects
53	Error Diffusion Dithering 1-Way		x		8/-/-/-/-	1k/2k/4k/8k		x
54	Error Diffusion Dithering 2-Way		x		8/-/-/-/-	1k/2k/4k/8k		x
55	OSD On Screen Display Character Map (OSD-CM) 2048 Characters Character/ Symbol Generator (OSD-CG)	x			8/-/-/-/-	1k/2k/4k/8k		
56	OSD Overlay Bitmap 1024x512 with 4x 32 Bit ARGB colors	x			8/-/-/-/-	1k/2k/4k/8k	x	x
57	OSD Overlay Bitmap 512x256 with 4x 32 Bit ARGB colors	x			8/-/-/-/-	1k/2k/4k/8k		x
58	OSD Overlay Bitmap 128x64 with 4x 32 Bit ARGB colors	x			8/-/-/-/-	1k/2k/4k/8k		x
59	Overlay with one graphical object selectable color, transparency and dimension (16384 Pixel)	x	x		8/-/-/-/-	1k/2k/4k/8k		x
60	Keystone Correction	x			8/10/12/-/-/-	1k/2k/-/-		x
61	Output Interface with FIFO for μC or DSP		x		8/10/12/16/20/32	1k/2k/4k/8k		x
62	Output Interface for TFT-Panel		x		8/10/12/-/-/-	1k/2k/4k/8k		x
63	Output Interface for DVI Transmitter		x		8/10/12/-/-/-	1k/2k/4k/8k	x	x
64	Output Interface with BT656-Syncs for video encoder		x		8/-/-/-/-	1k/2k/4k/8k		x
65	Output Interface with BT1120-Syncs		x		8/-/-/-/-	1k/2k/4k/8k		x
66	APIX TX Interface with Setup ROM	x	x					x
67	APIX RX Interface with Setup ROM	x	x					x
68	Image Sensor Setup and Capture			x			x	x
69	Parameter Inserting (selectable)	x	x		8/10/12/16/20/32			x
70	I2C Fast Framewise Configurator		x					x
71	I2C Slave with 1024 Byte Registermap		x				x	x
72	Testpattern Generator	x	x		8/10/12/16/20/32	1k/2k/4k/8k	x	x
73	Terminal style UART configuration			x			x	x
74	Simple DMA controller with one additional Wishbone	x					x	x
75	Accumulative DMA controller with one additional Wishbone	x					x	x
76	LUT DMA controller with one additional Wishbone	x					x	x
77	Port Watcher, DMA based	x						x
78	ID Register	x						x
79	System clock counter 64 Bit	x					x	x
80	Helion micro code sequencer		x					x
81	PWM output	x						x
82	Wishbone Memoryblock with external access port	x					x	x
83	Wishbone LUT with external access port and linear interpolation	x						x
84	Wishbone Slave Quadoutport 4x 32 Bit	x						x
85	Wishbone Slave Quadoutport 4x 32 Bit with extra port clock	x						x
86	Wishbone Slave Quadinport 4x 32 Bit	x						x
87	Wishbone Slave Singleoutport 32 Bit	x						x
88	Wishbone Slave Singleoutport 32 Bit with extra port clock	x						x
89	Wishbone Slave Singeinport 32 Bit	x						x
90	Wishbone Slave Octaoutport 8x 32 Bit	x						x
91	Wishbone Slave Octaoutport 8x 32 Bit with extra port clock	x						x
92	Wishbone Slave Octainport 8x 32 Bit	x						x
93	Wishbone Slave Hexaoutport 16x 32 Bit	x						x
94	Wishbone Slave Hexaoutport 16x 32 Bit with extra port clock	x					x	x
95	Wishbone Slave Hexainport 16x 32 Bit	x						x
96	Wishbone Slave Hexainhexaoutport 2x 16x 32 Bit	x						x
97	Wishbone Slave Hexainhexaoutport 2x 16x 32 Bit with extra port clock	x					x	x
98	Wishbone I2C Master						x	x
99	Wishbone I2C Slave with 256 Registers						x	x
100	Image Statistics, mono HDR	x			8/10/12/16/20/32	1k/2k/4k/8k	x	x
101	Image Statistic, RGB HDR, 4x4 fields	x			8/10/12/16/20/32	1k/2k/4k/8k		
102	Image Statistic, RGB HDR	x			8/10/12/16/20/32	1k/2k/4k/8k	x	x
103	Image Histogram	x			8/10/12/16/20/32	1k/2k/4k/8k	x	x
104	SDRAM based 4 port streaming memory controller		x		-/-/-/16/-/-	1k/-/-/-		x
105	DDR2 based 4 port streaming memory controller		x		-/-/-/16/-/-	1k/2k/4k/8k		x
106	SRAM based 4 port streaming memory controller		x		-/-/-/16/-/-	1k/-/-/-		x

IP-Licensing Options / Evaluation License

Procedure of SDK Evaluation (SDK = Test Drive) and Sample Source Code

Step 1
Trial (free of charge)

Kit is pre-loaded with demo bitstream
Customer can use the GUI (ICG) to setup AE, AWB, colors, contrast, gamma...

Step 2
In-depth evaluation (free of charge)

Customer has to sign free of charge **IONOS Evaluation License** by Lattice.
See also: Signing the evaluation IP licensing agreement with Lattice*
This License grants access to SW reference designs.
Customer can start first tests and developments (based on HDR-60).

Step 3
Preparation of product development and during development

Customer can buy prepaid support packages by Helion.
Support packages 01: Project Workshops
Support packages 02: Trainings (Sensor, ISP or FPGA)
Support packages 03: Consulting and Development
(Please contact: **sales@helionvision.com** for further information regarding the support packages)

Step 4
Production license once bitstream is finished for production. FPGA **piece based** license agreement by Lattice
or
Project license by Helion.

Signing the evaluation IP licensing agreement with Lattice *

Please send a mail to: sales@helionvision.com
Subject: Evaluation License HDR-60 - IONOS-ISP
Helion will forward your request to Lattice Semiconductors.

•Evaluation IP licensing:
By signing the evaluation IP licensing agreement with Lattice, customers will have access to Helion's complete IP suite at no cost. The IP suite includes documentation, **time-limited** IP cores and ISP pipeline example projects.

• Production IP licensing:
By signing the production IP licensing agreement with Lattice, customers keys are provided by Lattice to unlock the time limited IP-Cores. The License fee is part of the FPGA cost and not visible. The Helion IP is for use with Lattice special part number FPGA's.

Revision 20140801-v01

Revision History

Table 2.1: Revision History ICG Quick Start Guide

Date	Version	Section	Change Summary
2014-07-16	V01	-	Initial Release
2014-08-01	V01	-	Adaption of Licensing Options